REMARKS/ARGUMENTS

Applicants respectfully request further examination and reconsideration in view of the instant response. Claims 1, 3–9, 11–17 and 19–24 remain pending in the present case. Claims 1, 3–9, 11–17 and 19–24 are rejected. Claims 1, 9 and 17 are amended herein. No new matter has been added. Support for the amendments can be found in the instant specification at least on page 20, lines 24–34.

35 U.S.C. Section 103(a) Rejections

Claims 1, 3–9, 11–17 and 19–24

Per the instant Office Action, Claims 1, 3–9, 11–17 and 19–24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over United States Patent No. 5,357,517 by Takebe (hereinafter referred to as "Takebe") in view of in view of United States Patent No. 6,904,034 B2 by D. Kularatna et al., (hereinafter referred to as "Kularatna"). Claims 1, 9 and 17 are independent claims. Claims 3–8, 11–16 and 19–24 are dependent on independent Claims 1, 9 and 17, respectively, and include the recitations of independent Claims 1, 9 and 17, respectively. Hence, by demonstrating that Takebe and Kularatna do not show or suggest the limitations of Claims 1, 9 and 17, it is also demonstrated that Takebe and Kularatna do not show or suggest the embodiments of Claims 1, 9 and 17.

"As reiterated by the Supreme Court in *KSR*, the framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). Obviousness is a question of law based on underlying factual inquiries" including "[a]scertaining the differences between the claimed invention and the prior art" (MPEP 2141(II)). "In determining the differences between the prior art and the claims, the question under 35 U.S.C. 103 is not whether

the differences themselves would have been obvious, but whether the claimed invention as a whole would have been obvious" (emphasis in original; MPEP 2141.02(I)). Applicant notes that "[t]he prior art reference (or references when combined) need not teach or suggest all the claim limitations, however, Office personnel must explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art" (emphasis added; MPEP 2141(III)).

Applicants respectfully submit that the claims overcome the rejections under 35 U.S.C. §103, as the claims as a whole are neither taught nor suggested by Takebe and Kularatna, and that Office personnel have not explained why differences would have been obvious. Amended Independent Claim 1 recites (emphasis added),

> A method of error protection comprising:
> detecting an error during communication between nodes in a network, said nodes separated by a link;
> blocking further communication between said nodes in response to said detected error;
> unblocking said blocked communication between said nodes, provided said communicating nodes have resolved said detected error, wherein said communication between said nodes is re-enabled; and
> setting a link usage indicator in a first storage element by reach of said communicating nodes prior to communication therebetween, and wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element,
> wherein said resolving said detected error comprises generating a clearing bit from each of said communicating nodes, wherein said clearing bit clears a bit in said corresponding position.

Applicants respectfully submit that Takebe does not show, suggest, teach, or describe the embodiments of the claimed invention. Particularly, Takebe does not show or suggest, "setting a link usage indicator in a first storage element by reach of said communicating nodes prior to communication therebetween, and wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said

corresponding position in said first storage element," and "wherein said resolving said detected error comprises generating a clearing bit from each of said communicating nodes, wherein said clearing bit clears a bit in said corresponding position," as claimed. Applicants understand Takebe to teach a different way to store error indications, that is, "[s]ince it is so arranged that the storage content of temporary memory for temporarily storing therein a signal corresponding to the error content and the error position is not updated each time the error signal is inputted but updated intermittently according to an operator's instruction, even when errors frequently take place at a multiplicity of locations," [Abstract].

Applicants respectfully submit that Takebe teaches using a temporary memory for storing therein a signal, but does not among other things, teach or suggest "setting a link usage indicator in a first storage element by reach of said communicating nodes prior to communication therebetween, and wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element," and "wherein said resolving said detected error comprises generating a clearing bit from each of said communicating nodes, wherein said clearing bit clears a bit in said corresponding position (emphasis added) as claimed.

Applicants understand Takebe to use a clear indicator at said link when said data error is resolved. With reference to Fig. 1 of Takebe, the clear signal generating part 70 generates a clear signal CLR1 to the error counter 40 in accordance with the command received from the CPU 30 and inputs the signal CLR1 to the error counter 40. The clear signal generating part 75 similarly generates a clear signal CLR2 to the error kind register 45 and the error position register 50 in accordance with the

command received from the CPU 30 and in puts [sic] the signal CLR2 to these registers, [Col. 6, lines 15-23]. Also, Applicants understand Takebe to use error kind and position registers. More specifically, "in this mode, the data of the error kind and position registers 45 and 50 are kept at the previous data until the operator instructs it and when the operator instructs it, the registers are cleared," [col. 6, lines 40–42]. The Applicants respectfully submit that Takebe does not teach "generating a clearing bit from each of said communicating nodes, wherein said clearing bit clears a bit in said corresponding position," as claimed, but rather generates clear signals, CLR1 and CLR2, to the error counter, the error kind register, and the error position register.

Furthermore, Applicants respectfully submit that Kularatna does not overcome the shortcomings of Takebe. Applicants understand Kularatna to teach "a method and system for communicating data between a mobile communications architecture and a GPRS architecture, wherein each utilize a different mode of communication," [Column 2, lines 22–26]. Applicants respectfully submit that Kularatna teaches communications between architecture, but does not among other things, teach or suggest "setting a link usage indicator in a first storage element by reach of said communicating nodes prior to communication therebetween, and wherein each of said communicating nodes has a corresponding position in said first storage element, and wherein said link usage indicator set by each of said nodes is relative to said corresponding position in said first storage element," and "wherein said resolving said detected error comprises generating a clearing bit from each of said communicating nodes, wherein said clearing bit clears a bit in said corresponding position (emphasis added) as claimed.

As Takebe and Kularatna do not teach each and every claim limitation of Claim 1 (as discussed above), and as Office personnel have not explained why difference(s)

between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art, and as Claims 9 and 17 recite similar elements as Claim 1, Applicants respectfully submit that Claims 1, 9 and 17 overcome the 35 U.S.C. §103(a) rejection. As Claims 3–8, 11–16 and 19–24 are pending from an allowable base Claims and reciting additional features, Applicants respectfully submit that 3–8, 11–16 and 19–24 overcome the 35 U.S.C. §103(a) rejection. As such, Applicants respectfully submit that Claims 1, 3–9, 11–17 and 19–24 are allowable.

CONCLUSION

In light of the above remarks, Applicants respectfully request allowance of Claims 1, 3–9, 11–17 and 19–24.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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